WHAT IS CLAIMED IS:

1. A semiconductor device comprising a plurality of MOSFETs formed in a single semiconductor substrate,

each of the plurality of MOSFETs comprising:

a source region;

a drain region;

a channel forming region formed between the source region and the drain region;

an impurity region being added with an impurity having an opposite conductive type to said source region and said drain region and being formed under said channel forming region, and

wherein a concentration of the impurity in the channel forming region is from 1/100 to 1/10 of that in said impurity region.

2. A device according to claim 1, wherein the concentration of the impurity in the impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3.

3. A device according to claim 1,

wherein the concentration of the impurity in the impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3, and

wherein the impurity region is substantially not contact with the source region and the drain region.

4. A device according to claim 1, wherein the concentration of the impurity in the channel forming region is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3.

5. A method for producing a semiconductor device, said method comprising the steps

of:

preparing a single crystal semiconductor substrate;

introducing an impurity from a direction of the <110> axis with respect to said single crystal semiconductor substrate, said impurity comprising one selected from the 13 group or the 15 group,

forming an impurity region in the single crystal semiconductor substrate with a depth of from 20 to 150 nm by introducing the impurity,

wherein a concentration of the impurity in the single crystal semiconductor substrate within 10 nm from a surface thereof is from 1/100 to 1/10 of that in the impurity region.

6. A method for producing a semiconductor device comprising the steps of:

forming a gate insulating film and a gate electrode over a single crystal semiconductor substrate,

introducing an impurity selected from the 13 group or the 15 group from a direction of the <110> axis with respect to the single crystal semiconductor substrate, and

forming an impurity region in the single crystal semiconductor substrate with a depth of from 20 to 150 nm by introducing the impurity,

wherein a concentration of the impurity in the single crystal semiconductor substrate within 10 nm from a surface thereof is from 1/100 to 1/10 of that in said impurity region.

7. A method according to claim 6, wherein the step of forming said impurity region is carried out from two directions perpendicular to a longitudinal direction of said gate electrode.

8. A method according to claim 5, wherein the concentration of the impurity in the impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3.

9. A method according to claim 5, wherein the concentration of the impurity in the single crystal semiconductor substrate within 10 nm from a surface thereof is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3.

10. A method according to claim 5, wherein the step of introducing the impurity is carried out to an exposed surface of the single crystal semiconductor substrate.

11. A method according to claim 6, wherein the concentration of the impurity in the impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3.

12. A method according to claim 6, wherein the concentration of the impurity in the single crystal semiconductor substrate within 10 nm from a surface thereof is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3.

13. A method according to claim 6, wherein the step of introducing the impurity is carried out to an exposed surface of the single crystal semiconductor substrate.

14. A device according to claim 1, wherein each of the plurality of MOSFET further comprises a pair of LDD regions,

wherein one of the pair of LDD regions is formed between the source region and the channel forming region while the other of the pair of LDD regions is formed between the channel forming region and the drain region.

15. A device according to claim 1, wherein said semiconductor device is an integrated circuit (IC).

16. A method according to claim 5, wherein said semiconductor device is an integrated circuit (IC).

17. A method according to claim 6, wherein said semiconductor device is an integrated circuit (IC).

18. A device according to claim 1, wherein said semiconductor device is a microprocessor.

19. A method according to claim 5, wherein said semiconductor device is a microprocessor.

20. A method according to claim 6, wherein said semiconductor device is a microprocessor.

21. A device according to claim 18, wherein said microprocessor is at least one selected from the group consisting of a RISC processor and an ASIC processor.

22. A method according to claim 19, wherein said microprocessor is at least one selected from the group consisting of a RISC processor and an ASIC processor.

23. A method according to claim 20, wherein said microprocessor is at least one selected from the group consisting of a RISC processor and an ASIC processor.

24. A device according to claim 1, wherein said semiconductor device is at least one selected from the group consisting of a cellular phone, a personal handy phone system, and a portable computer.

25. A method according to claim 5, wherein said semiconductor device is at least one selected from the group consisting of a cellular phone, a personal handy phone system, and a portable computer.

26. A method according to claim 6, wherein said semiconductor device is at least one selected from the group consisting of a cellular phone, a personal handy phone system, and a portable computer.